APPLICATION

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METHOD FOR DETERMINING SEMICONDUCTOR OVERLAY ON GROUNDRULE DEVICES

Background Of The Invention

1. Field of the Invention

The present invention relates to the manufacture of integrated circuits and, in particular, to a method and system for determining overlay error between circuit layers made by a lithographic process.

2. Description of Related Art

Semiconductor manufacturing involves the printing of multiple integrated circuit patterns using lithographic methods on successive levels of exposure tools. A requirement of semiconductor manufacturing is to keep the alignment of each level to previous levels below product tolerance. Currently this is done using the optical microscope based tool that measures structures printed in the field kerf outside the product cell that comprises the printed circuit pattern. The field kerf is the area which separates the individual cells or patterns and which is unusable due to the width of the blade used to cut apart the cells or patterns upon completion of the printing. These structural features printed in the field kerf must be larger than the printed circuit pattern to enable the low resolution to image and make measurements of the current to prior level alignment.

Kerf to device overlay error prediction is an industry wide issue. A problem of conventional overlay metrology technique is that the printed structure used in the measurement is printed at a much larger size and different shape than that of the printed circuit. Due to the physics of optical lithography, mask making and the like, this can lead to errors in the measured structure overlay to that of the printed circuit overlay. In addition, typical high resolution methods of measuring in-chip overlay such as scanning electron microscopy (SEM) are complicated by the required direct placement of subsequent patterns on top of each other. This leads to difficulty or even impossibility of measuring the overlay directly in the product chip device since

the structures typically sit on top of each other and it may be difficult to discern an edge of a device feature on one level from an edge of a device feature on another level. At sub 0.3μm ground rules, the magnitude of the problem starts to become a potentially significant contribution to yield loss due to overlay error.

Bearing in mind the problems and deficiencies of the prior art, it is therefore an object of the present invention to provide an improved system and method for determining overlay error between different lithographically produced layers of an integrated circuit chip.

It is another object of the present invention to provide a system and method for determining overlay error between superimposed active circuit features on different lithographically produced layers of an integrated circuit chip.

A further object of the invention is to provide a system and method for determining overlay error that avoids the problem of discerning different superimposed active circuit features on different lithographically produced layers of an integrated circuit chip.

It is yet another object of the present invention to provide such a system and method for determining overlay error that does not reduce the amount of active circuit area on a semiconductor wafer.

Still other objects and advantages of the invention will in part be obvious and will in part be apparent from the specification.

Summary of the Invention

The above and other objects and advantages, which will be apparent to one of skill in the art, are achieved in the present invention which is directed to, in a first aspect, a method of determining overlay error in a desired direction in an integrated circuit made by a lithographic process. The method includes creating a first layer of the integrated circuit having at least one circuit area, the first layer circuit area including a first active circuit feature and a kerf area adjacent to the circuit area substantially free of active circuit features. The first layer kerf area includes a first measurement feature